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WHAT IS CLAIMED IS:

1. A system comprising:
 - N different memories wherein $N > 1$;
 - M different busses with each one of the busses having a bandwidth to transport data at a predetermined rate, operatively coupled to one of the N memories wherein M is greater than 1;
 - a plurality of memory controllers with each one of the plurality of memory controllers operatively coupled to one of the N memories, wherein said each one of the plurality of memory controllers setting an associated memory in a first mode or a second mode; and
 - an arbiter responsive to at least one memory request signal to generate an Access vector that causes information to be read simultaneously from multiple ones of the N memory set in the first mode wherein total bandwidth on the busses of the multiple ones of the N memories is greater than the bandwidth on a single bus of one of the N memories.
 2. The system of Claim 1 wherein the first mode includes a Read mode.
 3. The system of claims 1 or 2 wherein each of the N memories includes DDR DRAM.
 4. The system of claim 3 wherein each of the DDR DRAM are partitioned into at least four banks and at least one buffer spread across the at least four banks.

- 1 5. The system of claim 4 wherein each buffer is partitioned into multiple maskable units.
- 1 6. The system of claim 4 wherein each buffer is partitioned into four units.
- 1 7. The system of claim 6 wherein each unit is equivalent to 1/4 the size of the buffer.
- 1 8. The system of claim 6 wherein each unit is maskable.
- 1 9. The system of claim 1 wherein the arbiter includes a controller executing a slice selection algorithm comprising the steps of:
- Exclude slices scheduled for re-fresh cycle (indicated by each DRAM controller)
 - Assign slices for all R requests of Transmitter controller
 - Complement R-accesses from corresponding EPC queue [Slice; QW]
 - Assign slice to EPC for globally W excluded slices (e.g. slice is excluded by all slice exclusion rules from Receiver)
 - Assign slices to W requests in RR (Round Robin) fashion between non-excluded slices starting from last assigned slice (slice assigned to Receiver Controller in previous window)
 - Complement W-accesses by EPC accesses from corresponding EPC queue [Slice; QW] and
 - Assign slice to EPC requests according to priority expressed by Weight.

- 1 10. A system including:
- 2 a Network Processor including at least one Data Flow Chip, at least one Embedded
- 3 Processor Complex EPC chip, at least one Scheduler chip wherein the at least one EPC chip and
- 4 the at least one Scheduler chip are operatively coupled to the at least one Data Flow Chip;
- 5 a plurality of memory elements with each one coupled by a separate bus to the at least one
- 6 Data Flow Chip;
- 7 a first high speed data port that transmits data out of the Data Flow Chip; and
- 8 an arbiter operatively coupled to the Data Flow Chip, said arbiter being responsive to
- 9 Read (R) Requests to cause multiple ones of the bus to transmit data from associated memory
- 10 elements simultaneously wherein the combined data bandwidth on the multiple ones of the bus is
- 11 sufficient to meet Bandwidth requirements of the high speed port.
- 12 11. The system of claim 10 wherein the bandwidth on each bus includes approximately 7.75
- 13 Gbps.
- 14 12. The system of claim 10 or claim 11 wherein the bandwidth of the high speed port
- 15 includes approximately 10 Gbps.
- 16 13. The system of claim 10 further including a second high speed data port that transmits data
- 17 into the Data Flow Chip.

9 available simultaneously on respective busses associated with each one of the memory
10 elements.

- 1 25. A method including the acts of:
2 providing a plurality of separate memories in which data is stored;
3 receiving in an arbiter a request to read data from selected ones of said plurality of
4 separate memories; and
5 simultaneously reading said memories to provide data simultaneously on
6 individual busses coupled to the selected ones of said plurality of separate memories.
- 1 26. The method of claim 25 wherein the bandwidth of data on each individual bus is less than
2 the total bandwidth on activated busses.

- 1 27. A method comprising the acts of:
- 2 providing a plurality of separate memory modules in which frames from
- 3 communication devices can be stored;
- 4 partitioning a frame into multiple parts;
- 5 writing adjacent parts of the frame in different ones of the memory modules; and
- 6 simultaneously accessing multiple memory modules in a single memory access
- 7 window to read data therefrom wherein the total bandwidth of data output from the
- 8 multiple memory modules matches the bandwidth of a FAT pipe port on a
- 9 communication device.
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